IN THE CLAIMS

The status of the claims as presently amended is as follows:

1. (*Currently Amended*) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first well of a first conductivity type formed in the semiconductor substrate;

a second well of the first conductivity type formed in the semiconductor substrate, the first and second wells being discrete and spaced apart from each other;

a first lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said first well;

a second lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said second well; and

a punch-trough stopper area surrounding the source area and the drain area of said first lateral MOS transistor in the first well and providing a punch-through voltage resistance between said source area and said drain area of said first lateral MOS transistor,

wherein the punch-through stopper area is formed within the first well,

wherein said second lateral MOS transistor has a lower threshold voltage than said first lateral MOS transistor, and

wherein the length of the channel area of said first lateral MOS transistor is smaller than the length of the channel area of said second lateral MOS transistor.

2. (*Previously Amended*) The semiconductor integrated circuit device according to Claim 1, wherein said first lateral MOS transistor comprises a digital circuit device and said second MOS transistor comprises an analog circuit device.

3. (*Currently Amended*) ~~The~~A semiconductor integrated circuit device ~~according to Claim 1,~~ comprising:

a semiconductor substrate;

a first well of a first conductivity type formed in the semiconductor substrate;

a second well of the first conductivity type formed in the semiconductor substrate;

a first lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said first well;

a second lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said second well; and

a punch-trough stopper area surrounding the source area and the drain area of said first lateral MOS transistor in the first well and providing a punch-through voltage resistance between said source area and said drain area of said first lateral MOS transistor,

wherein said second lateral MOS transistor has a lower threshold voltage than said first lateral MOS transistor,

wherein the length of the channel area of said first lateral MOS transistor is smaller than the length of the channel area of said second lateral MOS transistor, and

wherein said second lateral MOS transistor has an offset drain area surrounding the drain area thereof and having a lower impurity concentration than the drain area thereof.

4. (*Previously Amended*) The semiconductor integrated circuit device according to Claim 3, further comprising a punch-through stopper area surrounding the source area of said second lateral MOS transistor and providing a punch-through voltage resistance between the source area of said second lateral MOS transistor and said offset drain area.

5. (*Original*) The semiconductor integrated circuit device according to any of Claims 1 to 4, further comprising a bipolar transistor integrated in said semiconductor substrate.

6. (*Original*) The semiconductor integrated circuit device according to any of Claims 1 to 4,

further comprising a diode integrated in said semiconductor substrate .

7. (*Original*) The semiconductor integrated circuit device according to any of Claims 1 to 4, further comprising a diffusion resistor integrated in said semiconductor substrate.

8. (*Currently Amended*) ~~The~~A semiconductor integrated circuit device ~~according to Claim 1,~~ comprising:

a semiconductor substrate;

a first well of a first conductivity type formed in the semiconductor substrate;

a second well of the first conductivity type formed in the semiconductor substrate;

a first lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said first well;

a second lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said second well; and

a punch-trough stopper area surrounding the source area and the drain area of said first lateral MOS transistor in the first well and providing a punch-through voltage resistance between said source area and said drain area of said first lateral MOS transistor,

wherein said second lateral MOS transistor has a lower threshold voltage than said first lateral MOS transistor,

wherein the length of the channel area of said first lateral MOS transistor is smaller than the length of the channel area of said second lateral MOS transistor, and

wherein said source area of said first lateral MOS transistor includes a source LDD area and said drain area of said of said first lateral MOS transistor includes a drain side LDD area, and wherein the punch-through stopper area has a pocket structure that encloses the source side LDD area and the drain side LDD area.

9-10. (*Canceled*)

11. (*Currently Amended*) ~~The~~A semiconductor integrated circuit device ~~according to Claim 1,~~ comprising:

a semiconductor substrate;

a first well of a first conductivity type formed in the semiconductor substrate;

a second well of the first conductivity type formed in the semiconductor substrate;

a first lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said first well;

a second lateral MOS transistor having a source area, a drain area, and a channel area formed between the source and drain areas thereof, the source, drain, and channel areas thereof being formed in said second well; and

a punch-trough stopper area surrounding the source area and the drain area of said first lateral MOS transistor in the first well and providing a punch-through voltage resistance between said source area and said drain area of said first lateral MOS transistor,

wherein said second lateral MOS transistor has a lower threshold voltage than said first lateral MOS transistor,

wherein the length of the channel area of said first lateral MOS transistor is smaller than the length of the channel area of said second lateral MOS transistor, and

wherein said first well has a lower impurity concentration than that of the punch-through stopper areas.